ADM-VB240 User Manual

Document Revision: 1.0
28th July 2026

	Head Office	US Office
Address:	160 Dundee Street, Edinburgh, EH11 1DQ, UK	10822 West Toller Drive, Suite 120, Deer Creek Technology Center, Littleton, CO 80127
Telephone:	+44 131 558 2600	(303) 954 8768
Email:	sales@alpha-data.com	sales@alpha-data.com
Website:	http://www.alpha-data.com	http://www.alpha-data.com

Table Of Contents

List of Tables

List of Figures

1 Introduction

The ADM-VB240 is a 3U VPX module. It includes an AMD Versal Premium device.

1.1 Key Features

Key Features

- 3U VPX form factor
- Adheres to OpenVPX 14.6.13-n slot profile
- Designed for Versal Premium Device VP2502 in the VSVB3340 package
- Alpha Data AVR based system monitor
- Two LPDDR4 memory interfaces, each with 64 bit wide data interface

1.2 References & Specifications

ANSI/VITA 46.0	*VPX Baseline Standard*, October 2007, VITA, ISBN 1-885731-44-2
ANSI/VITA 47.0	*Construction, Safety and Quality for Plug-In Modules Standard*, April 2019, VITA, ISBN 978-1-948739-08-5
ANSI/VITA 48.0	*Mechanical Specification for Microcomputers using Ruggedized Enhanced Design Implementation*, July 2020, VITA, ISBN 978-1-948739-20-7
ANSI/VITA 65.0	*OpenVPX System Specification*, June 2010, VITA, ISBN 1-885731-58-2
ANSI/VITA 66.0	*Optical Interconnect on VPX - Base Standard*, July 2016, VITA, ISBN 1-885731-90-6
AMD DS959	*Versal Premium Series Data Sheet: DC and AC Switching Characteristics*, June 2024, AMD
AMD AM002	*Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual*, October 2023, AMD
AMD AM010	*Versal Adaptive SoC SelectIO Resources Architecture Manual*, March 2024, AMD
AMD AM011	*Versal Adaptive SoC Technical Reference Manual*, October 2023, AMD
AMD AM017	*Versal ACAP GTM Transceivers Architecture Manual*, April 2022, AMD
AMD XAPP1375	*Simplified Power Sequencing*, August 2024, AMD
AMD UG863	*Versal Adaptive SoC PCB Design User Guide*, April 2024, AMD
AMD UG1304	*Versal ACAP System Software Developers Guide*, October 2021, AMD
ANSI/VITA 67.0	*Coaxial Interconnect on VPX - Base Standard*, September 2019, VITA, ISBN 978-1-948739-09-2
SOSA Edition 2.0*Technical Standard for SOSA Reference Architecture*	August 2023, The Open Group, ISBN 1-947754-85-0

Table 1 : References

1.3 Order Code

Order Code: **ADM-VB240/2MS/CC1**

See the https://alpha-data.com/xml//product_datasheets/ADM-VB240_v1.0.pdf datasheet for complete ordering options.

Figure 1 : ADM-VB240

1.4 Customizations

Alpha Data provides extensive customization options to existing commercial off-the-shelf (COTS) products.

Please contact **sales@alpha-data.com** to obtain a quote and start your project today.

2 Installation

2.1 Hardware Installation

2.1.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.2 Hardware Installation

2.2.1 System Requirements

The ADM-VB240 is a 3U VPX platform featuring the AMD Versal Premium XCVP2502 Adaptable SoC.

2.2.2 Cooling Requirements

The power dissipation of the board is highly dependent on the Adaptive SoC application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with AMD power estimation tools to determine the approximate current requirements for each power rail.

The board is supplied with a conduction cooled heatsink. It is the users responsibility to ensure the metalwork is appropriate for conduction cooled applications.

3 Board Information

3.1 Physical Specifications

The ADM-VB240 complies with VITA48.2 (3U / 160mm VPX).

Description	Measure
Total Dy	100.0 mm
Total Dx	160.0 mm
PCB Dx	157.70 mm
Total Dz	23.42 mm
Circuit assembly weight	TBD grams
Total weight (with heat sink)	TBD grams

Table 2 : Mechanical Dimensions

3.2 Chassis Requirements

3.2.1 Mechanical Requirements

A 3U VPX rack is required for mechanical compatibility.

3.2.2 Power Requirements

The ADM-VB240 is primarily powered via the +12V VPX power rail. The majority of internal power rails are generated from this rail.

The ADM-VB240 is capable of drawing up to 26A on the +12V VPX power rail.

The ADM-VB240 also requires the presence of a +3.3V_AUX auxiliary power rail, used to power the ACAP PMC, ACAP LPD, and on-board system monitoring and reset circuitry.

The ADM-VB240 is capable of drawing up to 1A on the +3.3V_AUX power rail.

Power consumption estimation requires the use of the AMD XPE spreadsheet (https://www.amd.com/en/products/adaptive-socs-and-fpgas/technologies/power-efficiency/power-estimator.html) and a power estimator tool available from Alpha Data. Please contact **support@alpha-data.com** to obtain this tool.

The power available to the rails calculated using XPE are as follows:

Voltage	Source Name	Current Capability
0.80	VCC_INT + VCC_PSFP + VCC_SOC + VCC_IO + VCC_RAM + VCCINT_GT	200A
0.92	MGTAVCC	25A
1.2	MGTAVTT	25A
1.1	VCCO + LPDDR4	8A
1.5	VCCAUX	8A

Table 3 : Available Power By Rail

4 Functional Description

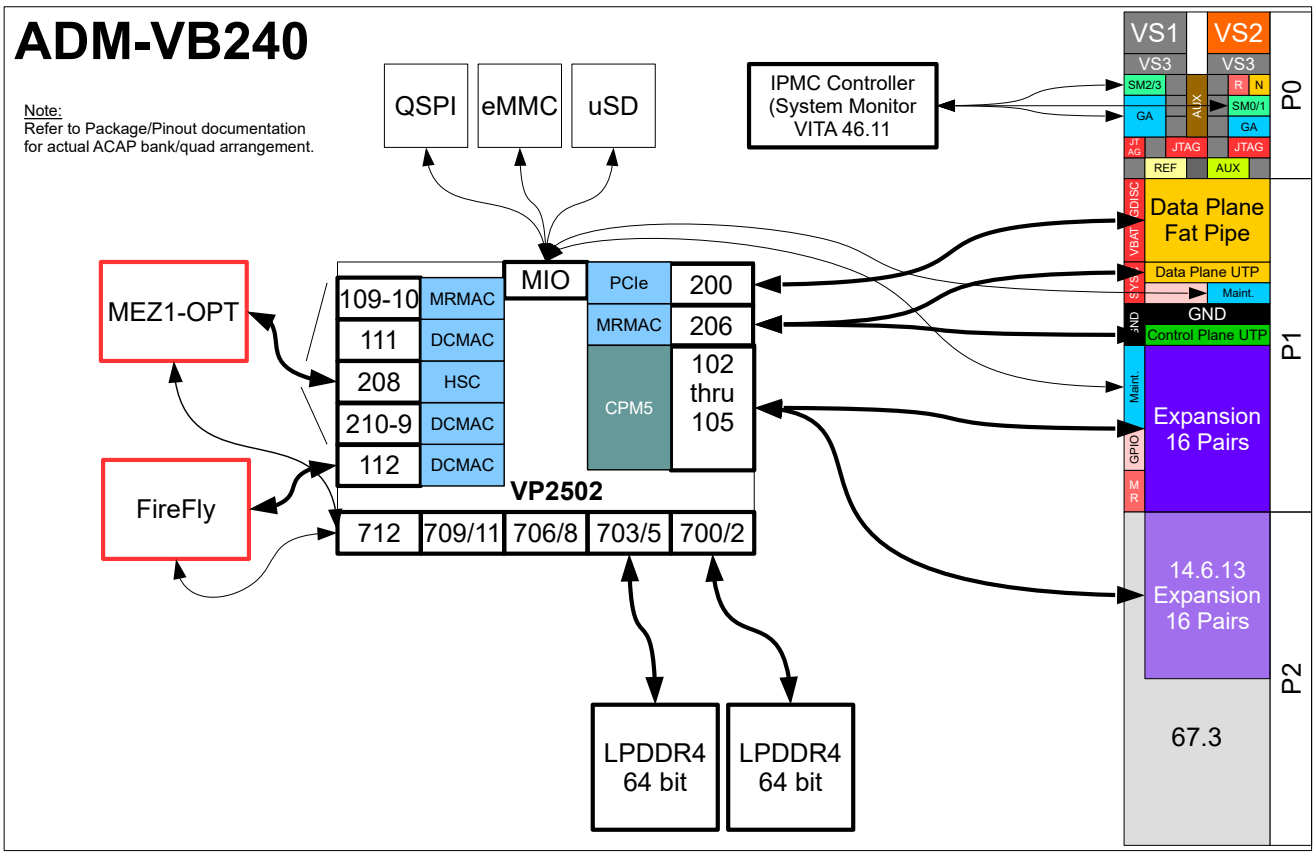

Figure 2 : Bank Diagram

4.1 Switch Definitions

Comp. Ref.	Function	ON State	Off State
SW1-1	ACAP MODE0	MODE0=LOW	MODE0=HIGH
SW1-2	ACAP MODE1	MODE1=LOW	MODE1=HIGH
SW1-3	ACAP MODE2	MODE2=LOW	MODE2=HIGH
SW1-4	ACAP MODE3	MODE3=LOW	MODE3=HIGH
SW1-5	POR_B	ACAP held in reset	ACAP reset released
SW1-6	VPX I2C0	IPMB-A I2C Disabled	Enabled
SW1-7	VPX I2C1	IPMB-B I2C Disabled	Enabled
SW1-8	Unused	n/a	n/a

Table 4 : Switch Definitions (SW1)

Comp. Ref.	Function	ON State	Off State
SW2-1	User Switch	Normal Operation	Normal Operation
SW2-2	User Switch	Normal Operation	Normal Operation
SW2-3	User Switch	Normal Operation	Normal Operation
SW2-4	PCIe REFCLK SEL	Internal	External (VPX)
SW2-5	JTAG select	Factory Use Only	Normal Operation
SW2-6	Unused	n/a	n/a
SW2-7	Service Mode	Enabled	Disabled
SW2-8	Unused	n/a	n/a

Table 5 : Switch Definitions (SW2)

4.2 LED Definitions

Comp. Ref.	Function	ON State	Off State
D2 (Green)	RS232 Rx	Activity	n/a
D3 (Green)	RS232 Tx	Activity	n/a
D4 (Amber)	JTAG select	VPX	Internal
D5 (Green)	System Monitor Status	See Table 12	
D6 (Red)	System Monitor Status	See Table 12	
D7 (Green)	Power Good	Power Good	Power Supplies off or fault detected
D8 (Red)	PS Error	PS Error	Normal Operation
D9 (Green)	Adaptive SoC (PL) Done	PL is configured	PL is not configured

Table 6 : Status LED Definitions

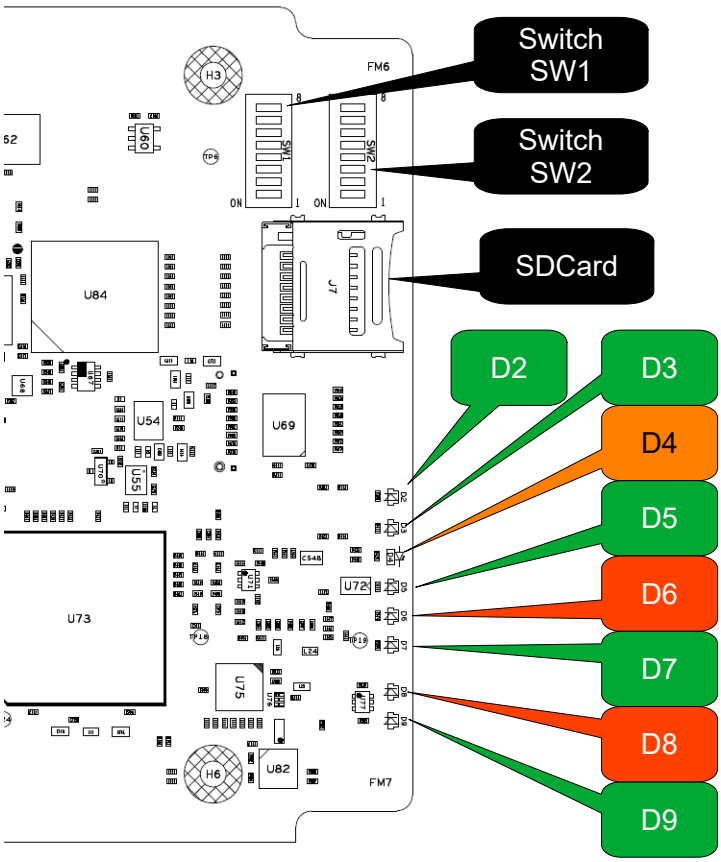

Figure 3 : Switches and LEDs

4.3 JTAG Interface

4.3.1 On-board Interface

The ACAP is the only on-board device in the JTAG chain.

The ACAP can be accesed over JTAG from the front USB-C connector.

Alternatively, JTAG access is possible from the backplane P0 interface (3.3V signal levels) when the USB-C interface is not in use.

4.4 ACAP

4.4.1 I/O Bank Voltages

The ACAP I/O is arranged in banks, each with its own supply pins. The bank numbers, their voltage, and function are shown below.

I/O Banks	Voltage	Purpose
500 (DIO)	1.8V	eMMC and QSPI
501 (MIO)	1.8V	SDIO and UART
502 (MIO)	1.8V	unused
503 (MIO)	3.3V	JTAG
700, 701, 702 (XPIO)	1.1V	LPDDR4
703, 704, 705 (XPIO)	1.1V	LPDDR4
706, 707, 708 (XPIO)	GND	unused
709, 710, 711 (XPIO)	GND	unused
712 (XPIO)	1.5V	GPIO and Clocks

Table 7 : Target FPGA I/O Banks

4.4.2 ACAP Processing System

4.4.2.1 Flash Memory

2x 2Gb Flash memory (Micron MT25QU02GCBB8E12-0SIT) devices are connected to the ACAP, and can be used to store configuration bitstreams.

4.4.2.2 SD Card

A micro SD card can be inserted into J7 and used to store configuration bitstreams.

The SD card interface uses SD_eMMC1, SD v2.0 Boot, interface of PMC MIO Bank 501.

4.4.2.3 eMMC

A 64GB eMMC device is connected to the ACAP, and can be used to store configuration bitstreams.

The eMMC interface uses SD_eMMC0, interface of PMC MIO Bank 500.

4.4.2.4 Boot Modes

MODE3 (SW1-4)	MODE2 (SW1-3)	MODE1 (SW1-2)	MODE0 (SW1-1)	Boot Mode
ON	ON	ON	ON	JTAG
ON	ON	ON	OFF	Quad SPI (24-bit addressing)
ON	ON	OFF	ON	Quad SPI (32-bit addressing)
OFF	OFF	OFF	ON	SD Flash - SD 3.0

Table 8 : Boot Mode Selection

Note: all other possible switch settings are reserved / invalid.

4.4.3 ACAP Programmable Logic

4.4.3.1 ACAP MGT Links

Quad	Destination	Hard IP
Quad	Destination	Hard IP
GTYP102-103	Expansion Plane 1 DFP	CPM5
GTYP104-105	Expansion Plane 2 DFP	CPM5
GTYP106	HSDP	HSDP
GTM109	Optics Module	MRMAC_X0Y2/DCMAC_X0Y2
GTM110	Optics Module	MRMAC_X0Y3/DCMAC_X0Y2
GTM111	Optics Module	DCMAC_X0Y2
GTM112	Firefly	DCMAC_X0Y2
GTYP200	Data Plane FP	PCIe_X1Y0/MRMAC_X1Y0
GTM206	Data Plane UTP and Control Plane UTP	MRMAC_X1Y1/DCMAC_X1Y0
GTM208	Optics Module	DCMAC_X1Y1
GTM209	Optics Module	DCMAC_X1Y1
GTM210	Optics Module	DCMAC_X1Y1

Table 9 : MGT Links

For MGT Clocking, please refer to Clocks.

4.4.3.2 Memory Interfaces

4.4.3.2.1 LPDDR4 SDRAM

The ADM-VB240 has two banks of LPDDR4 SDRAM.

Each bank consists of two 32-bit wide memory devices in parallel.

Micron MT53E2G32D4DE-046 IT are fitted as standard to provide 16GB per bank.

The memory banks are arranged for compatibility with the AMD Versal Memory Controllers in the XPIO banks.

4.5 Clocks

The clock routing on the ADM-VB240 is illustrated below.

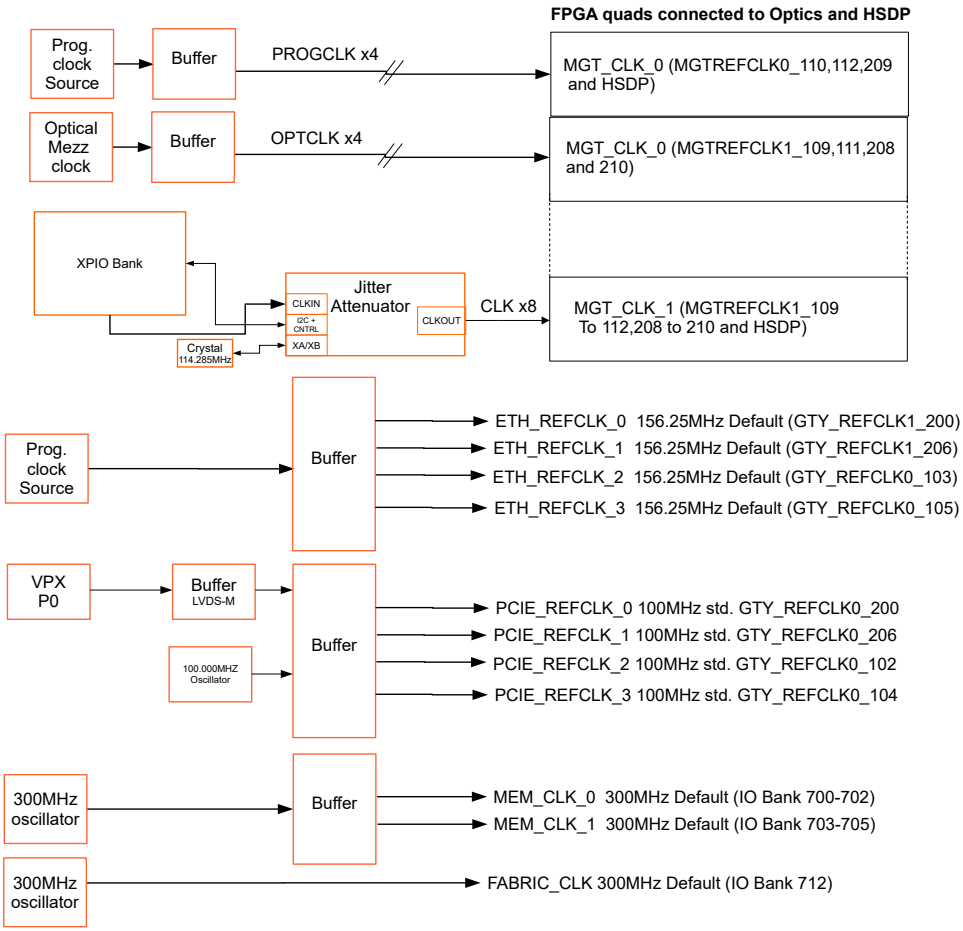

Figure 4 : Clocks

4.6 VPX P0 Interface

4.6.1 SYSRESET*

A buffered version of SYSRESET* connects to ACAP MIO38 and MIO39 (may be used as PCIe Reset).

A buffered version of SYSRESET* also connects to ACAP XPIO Bank 712 Pin BP58.

4.6.2 NVMRO

A buffered version of NVMRO connects to the QSPI Flash devices via a resistor fit option.

4.6.3 GDiscrete1

A buffered version of GDiscrete1 connects to ACAP XPIO Bank 712 Pin BM56.

4.6.4 MaskableReset

A buffered version of MaskableReset* connects to ACAP XPIO Bank 712 Pin BL54.

4.6.5 REF_CLK

A buffered version of REF_CLK+ connects to ACAP XPIO Bank 712 Pin BM54 (LVDS).

A buffered version of REF_CLK- connects to ACAP XPIO Bank 712 Pin BN54 (LVDS).

REF_CLK is terminated on the PCB.

4.6.6 AUX_CLK

A buffered version of AUX_CLK+ connects to ACAP XPIO Bank 712 Pin BK58 (LVDS).

A buffered version of AUX_CLK- connects to ACAP XPIO Bank 712 Pin BL57 (LVDS).

REF_CLK is terminated on the PCB.

4.6.7 I2C

4.6.7.1 Primary I2C

The Primary I2C Interface SM0/SM1 connects to the system monitor microcontroller.

The buffer enable pin is connected to switch SW1.6.

4.6.7.2 Secondary I2C

The Secondary I2C Interface SM2/SM3 connects to the system monitor microcontroller.

The buffer enable pin is connected to switch SW1.7.

4.7 VPX P1 Interfaces

4.7.1 HSSIO

Refer to the ACAP MGT Links section for details of the HSSIO connections.

4.7.2 VBAT

VBAT connects to the ACAP VCC_BATT pin via an LDO.

4.7.3 MP01

MP01 connects to the ACAP via buffering.

The MP01 buffer is enabled by pulling ACAP XPIO Bank 712 Pin BF54 low.

MP01_TD connects to ACAP XPIO Bank 712 Pin BE57.

MP01_RD connects to ACAP XPIO Bank 712 Pin BF57.

4.8 VPX P2 Interfaces

4.8.1 HSSIO

Refer to the ACAP MGT Links section for details of the HSSIO connections.

4.8.2 MP02

MP02 connects to the ACAP via buffering.

The MP02 buffer is enabled by pulling ACAP XPIO Bank 712 Pin BF54 low.

MP02_TD connects to ACAP XPIO Bank 712 Pin BE54.

MP02_RD connects to ACAP XPIO Bank 712 Pin BE55.

4.9 Optical Mezzanine Site

The ADM-VB240 includes an optical mezzanine site, please refer to the bank diagram for an overview of the connections.

Optical mezzanine cards are in an Alpha Data proprietary form factor. Please contact **sales@alpha-data.com** for more information.

4.9.1 Optical Mezzanine Site

The Optical Mezzanine site allows the connection of custom form factor boards intended to host optical modules.

4.9.1.1 Connectors

The Optical Mezzanine site consists of J1 and J6.

4.9.1.2 ACAP HSSIO

Six ACAP GTM transceiver quads are connected to the Optical Mezzanine Site.

Refer to ACAP MGT Links section for further details.

4.9.1.3 I2C

The I2C interfaces of the off-board optical modules connect to the ACAP HDIO via buffering.

SCL connects to ACAP HDIO Pin BP56.

SDA connects to ACAP HDIO Pin BP55.

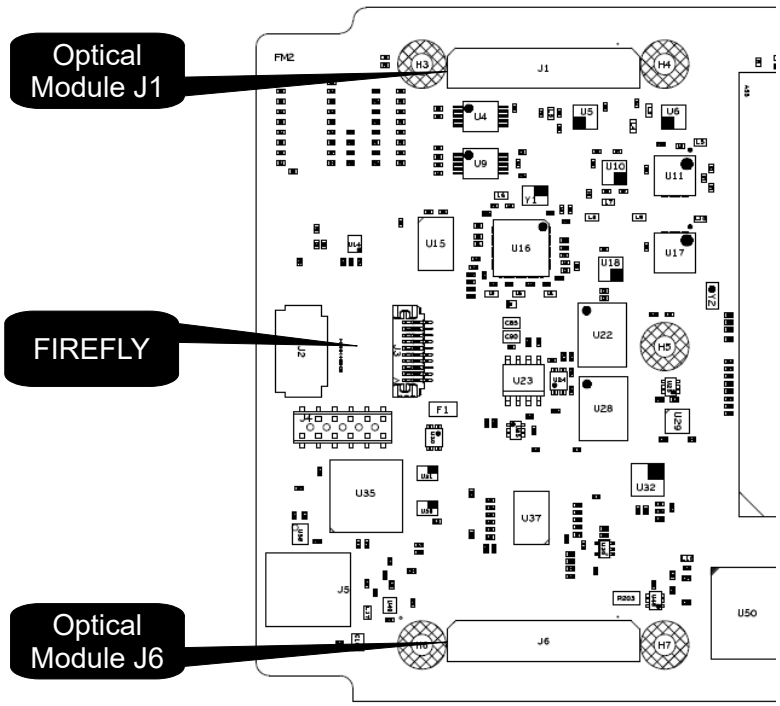

Figure 5 : Optical Connectors

4.10 Firefly Site

The ADM-VB240 allows the connection of a samtec Firefly optical module.

4.10.1 Connectors

The Samtec Module site consists of J2 and J3.

4.10.2 ACAP HSSIO

One ACAP transceiver quad is connected to the Samtec Site.

Refer to ACAP MGT Links section for further details.

4.10.3 I2C

The I2C interfaces and sideband signals of the Firefly module connect to the ACAP XPIO Bank 712 as follows:

SCL connects to ACAP Pin BN53.

SDA connects to ACAP Pin BP53.

MODPRS_L connects to ACAP Pin BU53.

MODSEL_L connects to ACAP Pin BU54.

INT_L connects to ACAP Pin BV53.

RESET_L connects to ACAP Pin BV54.

5 System Monitoring

The **ADM-VB240** has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using an Atmel AVR microcontroller (uC).

The microcontroller continually measures all voltage rails and temperature sensors and transmits the results to the ACAP, where they may be stored in blockram.

The following voltage rails and temperatures are monitored by the microcontroller:

Monitor	*Purpose*
12V0_VPX	12V VPX Supply Current
3V3_AUX	3V3_AUX VPX Supply Current
VCCINT	ACAP Core Supply Current
12V0_OM	Optical Module Supply Current
12V0_VPX	12V VPX Supply Voltage
3V3_AUX	3V3_AUX VPX Supply Voltage
1V8_DIG	1V8_DIG Internal Supply Voltage
3V3_DIG	3V3_DIG Internal Supply Voltage
1V5_DIG	1V5_DIG Internal Supply Voltage
MGT_AVCCAUX_1V5	ACAP MGT Aux Supply Voltage
MGT_1V2	ACAP MGT AVtt Supply Voltage
1V1_DIG	LPDDR4 SDRAM, ACAP I/O Voltage
MGT_0V92	ACAP MGT AVcc Supply Voltage
VCCINT	ACAP Core Supply Voltage
Temp1	microcontroller internal temperature
Temp2	TMP422 internal temperature
Temp3	FPGA on-die temperature (measured in TMP422)

Table 10 : Voltage and Temperature Monitors (in microcontroller)

The system monitor sensor values can be read via usb using the avr2util utility contained within the Alpha Data ADM-VB240 SDK.

5.1 Automatic Temperature Monitoring

The system monitor checks that the board and ACAP are being operated within the specified limits. If the temperature is close to the limit, a "Warning Alarm" interrupt is set.

If a limit is exceeded, a "Critical Alarm" interrupt is set. After the Critical Alarm is set, there is a 5 second delay before the system monitor unconfigures the FPGA by asserting its "PROG" pin.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang".

The temperature limits are shown in Table Temperature Limits. Note that the Min and Max values include a 5°C margin to prevent measurement errors triggering a false alarm.

	ACAP				Board (uC and PCB)			
	Min	Lower Warning	Upper Warning	Max	Min	Lower Warning	Upper Warning	Max
Industrial	-45°C	-35°C	+95°C	+105°C	-45°C	-35°C	+80°C	+90°C

Table 11 : Temperature Limits

5.2 System Monitor Status LEDs

LEDs D5 (Green) and D6 (Red) indicate the microcontroller status.

LEDs	*Status*
Flashing Green + Flashing Red (alternate)	Service Mode
Red	Missing application firmware or invalid firmware
Red + Green	Standby (Powered off)
Green	Running and no alarms
Flashing Green + Red	Attention - alarm active
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Red	FPGA configuration cleared to protect board

Table 12 : System Monitor Status LEDs

Appendix A: LPDDR4 Pinout

Pin Number	Signal Name
BM7	diff_clock_rtl_0_clk_n[0]
BL7	diff_clock_rtl_0_clk_p[0]
AY9	lpddr4_rtl_0_ca_a[0]
AY10	lpddr4_rtl_0_ca_a[1]
AV10	lpddr4_rtl_0_ca_a[2]
AT9	lpddr4_rtl_0_ca_a[3]
AW11	lpddr4_rtl_0_ca_a[4]
AW10	lpddr4_rtl_0_ca_a[5]
AT7	lpddr4_rtl_0_ca_b[0]
AW8	lpddr4_rtl_0_ca_b[1]
AW6	lpddr4_rtl_0_ca_b[2]
AW7	lpddr4_rtl_0_ca_b[3]
AY7	lpddr4_rtl_0_ca_b[4]
AY8	lpddr4_rtl_0_ca_b[5]
AY12	lpddr4_rtl_0_ck_c_a[0]
AU8	lpddr4_rtl_0_ck_c_b[0]
AW12	lpddr4_rtl_0_ck_t_a[0]
AU9	lpddr4_rtl_0_ck_t_b[0]
AR10	lpddr4_rtl_0_cke_a[0]
AT10	lpddr4_rtl_0_cke_a[1]
AV8	lpddr4_rtl_0_cke_b[0]
AU7	lpddr4_rtl_0_cke_b[1]
AR9	lpddr4_rtl_0_cs_a[0]
AV9	lpddr4_rtl_0_cs_a[1]
AW2	lpddr4_rtl_0_cs_b[0]
AR4	lpddr4_rtl_0_cs_b[1]
AP4	lpddr4_rtl_0_dmi_a[0]
BA10	lpddr4_rtl_0_dmi_a[1]
AW3	lpddr4_rtl_0_dmi_b[0]
BB3	lpddr4_rtl_0_dmi_b[1]
AV4	lpddr4_rtl_0_dq_a[0]
AW5	lpddr4_rtl_0_dq_a[1]
BB11	lpddr4_rtl_0_dq_a[10]
BA11	lpddr4_rtl_0_dq_a[11]

Table 13 : Bank 0 (continued on next page)

Pin Number	Signal Name
BB8	lpddr4_rtl_0_dq_a[12]
BC10	lpddr4_rtl_0_dq_a[13]
BC9	lpddr4_rtl_0_dq_a[14]
BC8	lpddr4_rtl_0_dq_a[15]
AU4	lpddr4_rtl_0_dq_a[2]
AV3	lpddr4_rtl_0_dq_a[3]
AT4	lpddr4_rtl_0_dq_a[4]
AU3	lpddr4_rtl_0_dq_a[5]
AR3	lpddr4_rtl_0_dq_a[6]
AP3	lpddr4_rtl_0_dq_a[7]
BB9	lpddr4_rtl_0_dq_a[8]
BA12	lpddr4_rtl_0_dq_a[9]
AP2	lpddr4_rtl_0_dq_b[0]
AV1	lpddr4_rtl_0_dq_b[1]
BA1	lpddr4_rtl_0_dq_b[10]
AY3	lpddr4_rtl_0_dq_b[11]
BC4	lpddr4_rtl_0_dq_b[12]
BB1	lpddr4_rtl_0_dq_b[13]
BB4	lpddr4_rtl_0_dq_b[14]
AY2	lpddr4_rtl_0_dq_b[15]
AU2	lpddr4_rtl_0_dq_b[2]
AW1	lpddr4_rtl_0_dq_b[3]
AU1	lpddr4_rtl_0_dq_b[4]
AT1	lpddr4_rtl_0_dq_b[5]
AR2	lpddr4_rtl_0_dq_b[6]
AT2	lpddr4_rtl_0_dq_b[7]
BA2	lpddr4_rtl_0_dq_b[8]
AY4	lpddr4_rtl_0_dq_b[9]
AT5	lpddr4_rtl_0_dqs_c_a[0]
BB13	lpddr4_rtl_0_dqs_c_a[1]
AP1	lpddr4_rtl_0_dqs_c_b[0]
BA4	lpddr4_rtl_0_dqs_c_b[1]
AR5	lpddr4_rtl_0_dqs_t_a[0]
BB14	lpddr4_rtl_0_dqs_t_a[1]
AN1	lpddr4_rtl_0_dqs_t_b[0]
BA5	lpddr4_rtl_0_dqs_t_b[1]

Table 13 : Bank 0 (continued on next page)

Pin Number	Signal Name
AV6	lpddr4_rtl_0_reset_n[0]
BG1	lpddr4_rtl_1_ca_a[0]
BF1	lpddr4_rtl_1_ca_a[1]
BJ1	lpddr4_rtl_1_ca_a[2]
BH1	lpddr4_rtl_1_ca_a[3]
BL2	lpddr4_rtl_1_ca_a[4]
BL1	lpddr4_rtl_1_ca_a[5]
BG9	lpddr4_rtl_1_ca_b[0]
BH9	lpddr4_rtl_1_ca_b[1]
BG7	lpddr4_rtl_1_ca_b[2]
BK8	lpddr4_rtl_1_ca_b[3]
BK9	lpddr4_rtl_1_ca_b[4]
BF7	lpddr4_rtl_1_ca_b[5]
BK3	lpddr4_rtl_1_ck_c_a[0]
BK10	lpddr4_rtl_1_ck_c_b[0]
BJ3	lpddr4_rtl_1_ck_t_a[0]
BJ10	lpddr4_rtl_1_ck_t_b[0]
BJ2	lpddr4_rtl_1_cke_a[0]
BG2	lpddr4_rtl_1_cke_a[1]
BH8	lpddr4_rtl_1_cke_b[0]
BG8	lpddr4_rtl_1_cke_b[1]
BF2	lpddr4_rtl_1_cs_a[0]
BK2	lpddr4_rtl_1_cs_a[1]
BF4	lpddr4_rtl_1_cs_b[0]
BG11	lpddr4_rtl_1_cs_b[1]
BF5	lpddr4_rtl_1_dmi_a[0]
BC13	lpddr4_rtl_1_dmi_a[1]
BG12	lpddr4_rtl_1_dmi_b[0]
BD3	lpddr4_rtl_1_dmi_b[1]
BL5	lpddr4_rtl_1_dq_a[0]
BJ5	lpddr4_rtl_1_dq_a[1]
BD8	lpddr4_rtl_1_dq_a[10]
BD7	lpddr4_rtl_1_dq_a[11]
BE9	lpddr4_rtl_1_dq_a[12]
BE8	lpddr4_rtl_1_dq_a[13]
BD12	lpddr4_rtl_1_dq_a[14]

Table 13 : Bank 0 (continued on next page)

Pin Number	Signal Name
BE11	lpddr4_rtl_1_dq_a[15]
BH4	lpddr4_rtl_1_dq_a[2]
BH5	lpddr4_rtl_1_dq_a[3]
BG4	lpddr4_rtl_1_dq_a[4]
BH3	lpddr4_rtl_1_dq_a[5]
BG3	lpddr4_rtl_1_dq_a[6]
BK5	lpddr4_rtl_1_dq_a[7]
BE13	lpddr4_rtl_1_dq_a[8]
BD11	lpddr4_rtl_1_dq_a[9]
BJ13	lpddr4_rtl_1_dq_b[0]
BF9	lpddr4_rtl_1_dq_b[1]
BB2	lpddr4_rtl_1_dq_b[10]
BE4	lpddr4_rtl_1_dq_b[11]
BE5	lpddr4_rtl_1_dq_b[12]
BE3	lpddr4_rtl_1_dq_b[13]
BE2	lpddr4_rtl_1_dq_b[14]
BD5	lpddr4_rtl_1_dq_b[15]
BH11	lpddr4_rtl_1_dq_b[2]
BF10	lpddr4_rtl_1_dq_b[3]
BH10	lpddr4_rtl_1_dq_b[4]
BJ11	lpddr4_rtl_1_dq_b[5]
BJ12	lpddr4_rtl_1_dq_b[6]
BK12	lpddr4_rtl_1_dq_b[7]
BC1	lpddr4_rtl_1_dq_b[8]
BD1	lpddr4_rtl_1_dq_b[9]
BL4	lpddr4_rtl_1_dqs_c_a[0]
BE10	lpddr4_rtl_1_dqs_c_a[1]
BF12	lpddr4_rtl_1_dqs_c_b[0]
BC5	lpddr4_rtl_1_dqs_c_b[1]
BK4	lpddr4_rtl_1_dqs_t_a[0]
BD10	lpddr4_rtl_1_dqs_t_a[1]
BF13	lpddr4_rtl_1_dqs_t_b[0]
BC6	lpddr4_rtl_1_dqs_t_b[1]
AV5	lpddr4_rtl_1_reset_n[0]

Table 13 : Bank 0

Pin Number	Signal Name
AU6	lpddr4_rtl_2_ca_a[0]
AT6	lpddr4_rtl_2_ca_a[1]
BT9	lpddr4_rtl_2_ca_a[2]
BT10	lpddr4_rtl_2_ca_a[3]
BP10	lpddr4_rtl_2_ca_a[4]
BV9	lpddr4_rtl_2_ca_a[5]
BM11	lpddr4_rtl_2_ca_b[0]
BN10	lpddr4_rtl_2_ca_b[1]
BP8	lpddr4_rtl_2_ca_b[2]
BU8	lpddr4_rtl_2_ca_b[3]
BN8	lpddr4_rtl_2_ca_b[4]
BM8	lpddr4_rtl_2_ca_b[5]
BR8	lpddr4_rtl_2_ck_c_a[0]
BR9	lpddr4_rtl_2_ck_c_b[0]
BL11	lpddr4_rtl_2_ck_t_a[0]
BN9	lpddr4_rtl_2_ck_t_b[0]
BL12	lpddr4_rtl_2_cke_a[0]
BM9	lpddr4_rtl_2_cke_a[1]
BL10	lpddr4_rtl_2_cke_b[0]
BL9	lpddr4_rtl_2_cke_b[1]
BU9	lpddr4_rtl_2_cs_a[0]
BP7	lpddr4_rtl_2_cs_a[1]
BV10	lpddr4_rtl_2_cs_b[0]
BR10	lpddr4_rtl_2_cs_b[1]
BR3	lpddr4_rtl_2_dmi_a[0]
BT5	lpddr4_rtl_2_dmi_a[1]
BK13	lpddr4_rtl_2_dmi_b[0]
BR5	lpddr4_rtl_2_dmi_b[1]
BU12	lpddr4_rtl_2_dq_a[0]
BR4	lpddr4_rtl_2_dq_a[1]
BG15	lpddr4_rtl_2_dq_a[10]
BF15	lpddr4_rtl_2_dq_a[11]
BN4	lpddr4_rtl_2_dq_a[12]
BN5	lpddr4_rtl_2_dq_a[13]
BT6	lpddr4_rtl_2_dq_a[14]
BV5	lpddr4_rtl_2_dq_a[15]

Table 14 : Bank 1 (continued on next page)

Pin Number	Signal Name
BU6	lpddr4_rtl_2_dq_a[14]
BV6	lpddr4_rtl_2_dq_a[15]
BE14	lpddr4_rtl_2_dq_a[2]
BH15	lpddr4_rtl_2_dq_a[3]
BM12	lpddr4_rtl_2_dq_a[4]
BM13	lpddr4_rtl_2_dq_a[5]
BM14	lpddr4_rtl_2_dq_a[6]
BL14	lpddr4_rtl_2_dq_a[7]
BM3	lpddr4_rtl_2_dq_a[8]
BM4	lpddr4_rtl_2_dq_a[9]
BU11	lpddr4_rtl_2_dq_b[0]
BV13	lpddr4_rtl_2_dq_b[1]
BP1	lpddr4_rtl_2_dq_b[10]
BN1	lpddr4_rtl_2_dq_b[11]
BN3	lpddr4_rtl_2_dq_b[12]
BP3	lpddr4_rtl_2_dq_b[13]
BU4	lpddr4_rtl_2_dq_b[14]
BT4	lpddr4_rtl_2_dq_b[15]
BV11	lpddr4_rtl_2_dq_b[2]
BV14	lpddr4_rtl_2_dq_b[3]
BR12	lpddr4_rtl_2_dq_b[4]
BR13	lpddr4_rtl_2_dq_b[5]
BT12	lpddr4_rtl_2_dq_b[6]
BT11	lpddr4_rtl_2_dq_b[7]
BR2	lpddr4_rtl_2_dq_b[8]
BP2	lpddr4_rtl_2_dq_b[9]
BD15	lpddr4_rtl_2_dqs_c_a[0]
BP5	lpddr4_rtl_2_dqs_c_a[1]
BP13	lpddr4_rtl_2_dqs_c_b[0]
BM1	lpddr4_rtl_2_dqs_c_b[1]
BD14	lpddr4_rtl_2_dqs_t_a[0]
BP6	lpddr4_rtl_2_dqs_t_a[1]
BP12	lpddr4_rtl_2_dqs_t_b[0]
BM2	lpddr4_rtl_2_dqs_t_b[1]
BR7	lpddr4_rtl_2_reset_n[0]
BV19	lpddr4_rtl_3_ca_a[0]

Table 14 : Bank 1 (continued on next page)

Pin Number	Signal Name
BV18	lpddr4_rtl_3_ca_a[1]
BV21	lpddr4_rtl_3_ca_a[2]
BV20	lpddr4_rtl_3_ca_a[3]
BT19	lpddr4_rtl_3_ca_a[4]
BT20	lpddr4_rtl_3_ca_a[5]
BJ20	lpddr4_rtl_3_ca_b[0]
BJ21	lpddr4_rtl_3_ca_b[1]
BM22	lpddr4_rtl_3_ca_b[2]
BK22	lpddr4_rtl_3_ca_b[3]
BJ22	lpddr4_rtl_3_ca_b[4]
BL22	lpddr4_rtl_3_ca_b[5]
BU17	lpddr4_rtl_3_ck_c_a[0]
BH21	lpddr4_rtl_3_ck_c_b[0]
BT17	lpddr4_rtl_3_ck_t_a[0]
BH20	lpddr4_rtl_3_ck_t_b[0]
BT21	lpddr4_rtl_3_cke_a[0]
BU19	lpddr4_rtl_3_cke_a[1]
BK18	lpddr4_rtl_3_cke_b[0]
BJ18	lpddr4_rtl_3_cke_b[1]
BU18	lpddr4_rtl_3_cs_a[0]
BU21	lpddr4_rtl_3_cs_a[1]
BP20	lpddr4_rtl_3_cs_b[0]
BF21	lpddr4_rtl_3_cs_b[1]
BN20	lpddr4_rtl_3_dmi_a[0]
BD17	lpddr4_rtl_3_dmi_a[1]
BE20	lpddr4_rtl_3_dmi_b[0]
BT15	lpddr4_rtl_3_dmi_b[1]
BR22	lpddr4_rtl_3_dq_a[0]
BT22	lpddr4_rtl_3_dq_a[1]
BF16	lpddr4_rtl_3_dq_a[10]
BJ16	lpddr4_rtl_3_dq_a[11]
BM17	lpddr4_rtl_3_dq_a[12]
BL17	lpddr4_rtl_3_dq_a[13]
BH16	lpddr4_rtl_3_dq_a[14]
BG17	lpddr4_rtl_3_dq_a[15]
BP22	lpddr4_rtl_3_dq_a[2]

Table 14 : Bank 1 (continued on next page)

Pin Number	Signal Name
BP21	lpddr4_rtl_3_dq_a[3]
BP18	lpddr4_rtl_3_dq_a[4]
BR20	lpddr4_rtl_3_dq_a[5]
BR19	lpddr4_rtl_3_dq_a[6]
BP17	lpddr4_rtl_3_dq_a[7]
BJ15	lpddr4_rtl_3_dq_a[8]
BE16	lpddr4_rtl_3_dq_a[9]
BD20	lpddr4_rtl_3_dq_b[0]
BF19	lpddr4_rtl_3_dq_b[1]
BU16	lpddr4_rtl_3_dq_b[10]
BV16	lpddr4_rtl_3_dq_b[11]
BV15	lpddr4_rtl_3_dq_b[12]
BU14	lpddr4_rtl_3_dq_b[13]
BR15	lpddr4_rtl_3_dq_b[14]
BR14	lpddr4_rtl_3_dq_b[15]
BG20	lpddr4_rtl_3_dq_b[2]
BF22	lpddr4_rtl_3_dq_b[3]
BG21	lpddr4_rtl_3_dq_b[4]
BF18	lpddr4_rtl_3_dq_b[5]
BE22	lpddr4_rtl_3_dq_b[6]
BD21	lpddr4_rtl_3_dq_b[7]
BT14	lpddr4_rtl_3_dq_b[8]
BP16	lpddr4_rtl_3_dq_b[9]
BR18	lpddr4_rtl_3_dqs_c_a[0]
BK17	lpddr4_rtl_3_dqs_c_a[1]
BE19	lpddr4_rtl_3_dqs_c_b[0]
BP15	lpddr4_rtl_3_dqs_c_b[1]
BR17	lpddr4_rtl_3_dqs_t_a[0]
BJ17	lpddr4_rtl_3_dqs_t_a[1]
BD18	lpddr4_rtl_3_dqs_t_b[0]
BN15	lpddr4_rtl_3_dqs_t_b[1]
BT7	lpddr4_rtl_3_reset_n[0]

Table 14 : Bank 1

Appendix B: Backplane HSSIO Quad Mapping

ACAP Quad	Lane	Signal Name
102	0	EP15
102	1	EP14
102	2	EP13
102	3	EP12
103	0	EP11
103	1	EP10
103	2	EP09
103	3	EP08
104	0	EP07
104	1	EP06
104	2	EP05
104	3	EP04
105	0	EP03
105	1	EP02
105	2	EP01
105	3	EP00
200	0	DP00
200	1	DP01
200	2	DP02
200	3	DP03
206	0	DPUTP01
206	1	CPUTP01

Table 15 : Backplane HSSIO Quad Mapping

Appendix C: Optical HSSIO Quad Mapping

ACAP Quad	Lanes	Signal Name
109	[3:0]	OMFP0[3:0]
110	[3:0]	OMFP1[3:0]
111	[3:0]	OMFP2[3:0]
208	[3:0]	OMFP3[3:0]
209	[3:0]	OMFP4[3:0]
210	[3:0]	OMFP5[3:0]

Table 16 : Optical Mezzanine HSSIO Quad Mapping

ACAP Quad	Lanes	Signal Name
112	[3:0]	FF[3:0]

Table 17 : Firefly Module Quad Mapping

Appendix D: ACAP MIO Pin Assignment

MIO Pin	Controller	Signal
0	QSPI 8b Boot	CLK0
1	QSPI 8b Boot	IO0 1
2	QSPI 8b Boot	IO0 2
3	QSPI 8b Boot	IO0 3
4	QSPI 8b Boot	IO0 0
5	QSPI 8b Boot	CS0
6	-	-
7	QSPI 8b Boot	CS1
8	QSPI 8b Boot	IO1 0
9	QSPI 8b Boot	IO1 1
10	QSPI 8b Boot	IO1 2
11	QSPI 8b Boot	IO1 3
12	QSPI 8b Boot	CLK1
13	eMMC	eMMC_D0
14	eMMC	eMMC_D1
15	eMMC	eMMC_D2
16	eMMC	eMMC_D3
17	eMMC	eMMC_RST_N
18	eMMC	eMMC_CLK
19	eMMC	eMMC_D4
20	eMMC	eMMC_D5
21	eMMC	eMMC_D6
22	eMMC	eMMC_D7
23	eMMC	eMMC_CMD
24	-	-
25	-	-

Table 18 : PMC MIO Bank 500

MIO Pin	Controller	Signal
26	SD_eMMC_1	CLK
27	-	-
28	-	-
29	SD_eMMC_1	CMD
30	SD_eMMC_1	D 0
31	SD_eMMC_1	D 1
32	SD_eMMC_1	D 2
33	SD_eMMC_1	D 3
34	-	-
35	-	-
36	-	-
37	-	-
38	PCIe Resets	RST 0
39	PCIe Resets	RST 1
40	-	-
41	-	-
42	UART0	RXD
43	UART1	RXD
44	-	-
45	-	-
46	-	-
47	-	-
48	-	-
49	PMC_SMON_SCL	ERROR
50	PMC_SMON_SDA	ERROR
51	-	-

Table 19 : PMC MIO Bank 501

MIO Pin	Controller	Signal
0..25	-	-

Table 20 : LPD MIO Bank 502 (unused)

Appendix E: ACAP Pin Assignments

ACAP Pin	Signal
BP57	AVR_B2U_1V5
BR55	AVR_MON_CLK_1V5
BR57	AVR_U2B_1V5
H57	CPUTP01-RD-N
H56	CPUTP01-RD-P
R54	CPUTP01-TD-N
R53	CPUTP01-TD-P
A27	DONE
BC56	DP01-RD0_N
BC55	DP01-RD0_P
BB58	DP01-RD1_N
BB57	DP01-RD1_P
BA56	DP01-RD2_N
BA55	DP01-RD2_P
AY58	DP01-RD3_N
AY57	DP01-RD3_P
BC53	DP01-TD0_N
BC52	DP01-TD0_P
BC49	DP01-TD1_N
BC48	DP01-TD1_P
BB51	DP01-TD2_N
BB50	DP01-TD2_P
BA53	DP01-TD3_N
BA52	DP01-TD3_P
K57	DPUTP01-RD-N
K56	DPUTP01-RD-P
U54	DPUTP01-TD-N
U53	DPUTP01-TD-P
L22	EMMC_CLK
M21	EMMC_CMD
J23	eMMC_D0
K23	eMMC_D1
M23	eMMC_D2
N23	eMMC_D3

Table 21 : All ACAP Pins (continued on next page)

ACAP Pin	Signal
K22	eMMC_D4
J22	eMMC_D5
G22	eMMC_D6
G21	eMMC_D7
M22	eMMC_RST_N
L1	EP00-RD_N
L2	EP00-RD_P
T4	EP00-TD_N
T5	EP00-TD_P
N1	EP01-RD_N
N2	EP01-RD_P
U6	EP01-TD_N
U7	EP01-TD_P
R1	EP02-RD_N
R2	EP02-RD_P
V4	EP02-TD_N
V5	EP02-TD_P
U1	EP03-RD_N
U2	EP03-RD_P
W6	EP03-TD_N
W7	EP03-TD_P
W1	EP04-RD_N
W2	EP04-RD_P
AA6	EP04-TD_N
AA7	EP04-TD_P
Y3	EP05-RD_N
Y4	EP05-RD_P
AC6	EP05-TD_N
AC7	EP05-TD_P
AA1	EP06-RD_N
AA2	EP06-RD_P
AE6	EP06-TD_N
AE7	EP06-TD_P
AB3	EP07-RD_N
AB4	EP07-RD_P
AF8	EP07-TD_N

Table 21 : All ACAP Pins (continued on next page)

ACAP Pin	Signal
AF9	EP07-TD_P
AC1	EP08-RD_N
AC2	EP08-RD_P
AG6	EP08-TD_N
AG7	EP08-TD_P
AD3	EP09-RD_N
AD4	EP09-RD_P
AH8	EP09-TD_N
AH9	EP09-TD_P
AE1	EP10-RD_N
AE2	EP10-RD_P
AJ6	EP10-TD_N
AJ7	EP10-TD_P
AF3	EP11-RD_N
AF4	EP11-RD_P
AK4	EP11-TD_N
AK5	EP11-TD_P
AG1	EP12-RD_N
AG2	EP12-RD_P
AL6	EP12-TD_N
AL7	EP12-TD_P
AH3	EP13-RD_N
AH4	EP13-RD_P
AM8	EP13-TD_N
AM9	EP13-TD_P
AJ1	EP14-RD_N
AJ2	EP14-RD_P
AM4	EP14-TD_N
AM5	EP14-TD_P
AL1	EP15-RD_N
AL2	EP15-RD_P
AN6	EP15-TD_N
AN7	EP15-TD_P
C26	ERROR_OUT
AN10	ETHCLK0_N
AN11	ETHCLK0_P

Table 21 : All ACAP Pins (continued on next page)

ACAP Pin	Signal
AE10	ETHCLK1_N
AE11	ETHCLK1_P
AY47	ETHCLK2_N
AY46	ETHCLK2_P
AD47	ETHCLK3_N
AD46	ETHCLK3_P
BV53	FF_INT_L_1V5
BU53	FF_MODPRS_L_1V5
BU54	FF_MODSEL_L_1V5
BV54	FF_RESET_L_1V5
D16	FF_RX0_N
E16	FF_RX0_P
B17	FF_RX1_N
C17	FF_RX1_P
D18	FF_RX2_N
E18	FF_RX2_P
B19	FF_RX3_N
C19	FF_RX3_P
BP53	FF_SCL_1V5
BN53	FF_SDA_1V5
G17	FF_TX0_N
H17	FF_TX0_P
J18	FF_TX1_N
K18	FF_TX1_P
G19	FF_TX2_N
H19	FF_TX2_P
J20	FF_TX3_N
K20	FF_TX3_P
K3	HSDP_RX_N
K4	HSDP_RX_P
R6	HSDP_TX_N
R7	HSDP_TX_P
W10	JACLK0_N
W11	JACLK0_P
T8	JACLK1_N
T9	JACLK1_P

Table 21 : All ACAP Pins (continued on next page)

ACAP Pin	Signal
P8	JACLK2_N
P9	JACLK2_P
M8	JACLK3_N
M9	JACLK3_P
Y51	JACLK4_N
Y50	JACLK4_P
V51	JACLK5_N
V50	JACLK5_P
T51	JACLK6_N
T50	JACLK6_P
AA10	JACLK7_N
AA11	JACLK7_P
A26	JTAG_ACAP_TCK
D27	JTAG_ACAP_TDI
D28	JTAG_ACAP_TDO
B26	JTAG_ACAP_TMS
AY9	lpddr4_rtl_0_ca_a[0]
AY10	lpddr4_rtl_0_ca_a[1]
AV10	lpddr4_rtl_0_ca_a[2]
AT9	lpddr4_rtl_0_ca_a[3]
AW11	lpddr4_rtl_0_ca_a[4]
AW10	lpddr4_rtl_0_ca_a[5]
AT7	lpddr4_rtl_0_ca_b[0]
AW8	lpddr4_rtl_0_ca_b[1]
AW6	lpddr4_rtl_0_ca_b[2]
AW7	lpddr4_rtl_0_ca_b[3]
AY7	lpddr4_rtl_0_ca_b[4]
AY8	lpddr4_rtl_0_ca_b[5]
AY12	lpddr4_rtl_0_ck_c_a[0]
AU8	lpddr4_rtl_0_ck_c_b[0]
AW12	lpddr4_rtl_0_ck_t_a[0]
AU9	lpddr4_rtl_0_ck_t_b[0]
AR10	lpddr4_rtl_0_cke_a[0]
AT10	lpddr4_rtl_0_cke_a[1]
AV8	lpddr4_rtl_0_cke_b[0]
AU7	lpddr4_rtl_0_cke_b[1]

Table 21 : All ACAP Pins (continued on next page)

ACAP Pin	Signal
AR9	lpddr4_rtl_0_cs_a[0]
AV9	lpddr4_rtl_0_cs_a[1]
AW2	lpddr4_rtl_0_cs_b[0]
AR4	lpddr4_rtl_0_cs_b[1]
AP4	lpddr4_rtl_0_dmi_a[0]
BA10	lpddr4_rtl_0_dmi_a[1]
AW3	lpddr4_rtl_0_dmi_b[0]
BB3	lpddr4_rtl_0_dmi_b[1]
AV4	lpddr4_rtl_0_dq_a[0]
AW5	lpddr4_rtl_0_dq_a[1]
BB11	lpddr4_rtl_0_dq_a[10]
BA11	lpddr4_rtl_0_dq_a[11]
BB8	lpddr4_rtl_0_dq_a[12]
BC10	lpddr4_rtl_0_dq_a[13]
BC9	lpddr4_rtl_0_dq_a[14]
BC8	lpddr4_rtl_0_dq_a[15]
AU4	lpddr4_rtl_0_dq_a[2]
AV3	lpddr4_rtl_0_dq_a[3]
AT4	lpddr4_rtl_0_dq_a[4]
AU3	lpddr4_rtl_0_dq_a[5]
AR3	lpddr4_rtl_0_dq_a[6]
AP3	lpddr4_rtl_0_dq_a[7]
BB9	lpddr4_rtl_0_dq_a[8]
BA12	lpddr4_rtl_0_dq_a[9]
AP2	lpddr4_rtl_0_dq_b[0]
AV1	lpddr4_rtl_0_dq_b[1]
BA1	lpddr4_rtl_0_dq_b[10]
AY3	lpddr4_rtl_0_dq_b[11]
BC4	lpddr4_rtl_0_dq_b[12]
BB1	lpddr4_rtl_0_dq_b[13]
BB4	lpddr4_rtl_0_dq_b[14]
AY2	lpddr4_rtl_0_dq_b[15]
AU2	lpddr4_rtl_0_dq_b[2]
AW1	lpddr4_rtl_0_dq_b[3]
AU1	lpddr4_rtl_0_dq_b[4]
AT1	lpddr4_rtl_0_dq_b[5]

Table 21 : All ACAP Pins (continued on next page)

ACAP Pin	Signal
AR2	lpddr4_rtl_0_dq_b[6]
AT2	lpddr4_rtl_0_dq_b[7]
BA2	lpddr4_rtl_0_dq_b[8]
AY4	lpddr4_rtl_0_dq_b[9]
AT5	lpddr4_rtl_0_dqs_c_a[0]
BB13	lpddr4_rtl_0_dqs_c_a[1]
AP1	lpddr4_rtl_0_dqs_c_b[0]
BA4	lpddr4_rtl_0_dqs_c_b[1]
AR5	lpddr4_rtl_0_dqs_t_a[0]
BB14	lpddr4_rtl_0_dqs_t_a[1]
AN1	lpddr4_rtl_0_dqs_t_b[0]
BA5	lpddr4_rtl_0_dqs_t_b[1]
AV6	lpddr4_rtl_0_reset_n[0]
BG1	lpddr4_rtl_1_ca_a[0]
BF1	lpddr4_rtl_1_ca_a[1]
BJ1	lpddr4_rtl_1_ca_a[2]
BH1	lpddr4_rtl_1_ca_a[3]
BL2	lpddr4_rtl_1_ca_a[4]
BL1	lpddr4_rtl_1_ca_a[5]
BG9	lpddr4_rtl_1_ca_b[0]
BH9	lpddr4_rtl_1_ca_b[1]
BG7	lpddr4_rtl_1_ca_b[2]
BK8	lpddr4_rtl_1_ca_b[3]
BK9	lpddr4_rtl_1_ca_b[4]
BF7	lpddr4_rtl_1_ca_b[5]
BK3	lpddr4_rtl_1_ck_c_a[0]
BK10	lpddr4_rtl_1_ck_c_b[0]
BJ3	lpddr4_rtl_1_ck_t_a[0]
BJ10	lpddr4_rtl_1_ck_t_b[0]
BJ2	lpddr4_rtl_1_cke_a[0]
BG2	lpddr4_rtl_1_cke_a[1]
BH8	lpddr4_rtl_1_cke_b[0]
BG8	lpddr4_rtl_1_cke_b[1]
BF2	lpddr4_rtl_1_cs_a[0]
BK2	lpddr4_rtl_1_cs_a[1]
BF4	lpddr4_rtl_1_cs_b[0]

Table 21 : All ACAP Pins (continued on next page)

ACAP Pin	Signal
BG11	lpddr4_rtl_1_cs_b[1]
BF5	lpddr4_rtl_1_dmi_a[0]
BC13	lpddr4_rtl_1_dmi_a[1]
BG12	lpddr4_rtl_1_dmi_b[0]
BD3	lpddr4_rtl_1_dmi_b[1]
BL5	lpddr4_rtl_1_dq_a[0]
BJ5	lpddr4_rtl_1_dq_a[1]
BD8	lpddr4_rtl_1_dq_a[10]
BD7	lpddr4_rtl_1_dq_a[11]
BE9	lpddr4_rtl_1_dq_a[12]
BE8	lpddr4_rtl_1_dq_a[13]
BD12	lpddr4_rtl_1_dq_a[14]
BE11	lpddr4_rtl_1_dq_a[15]
BH4	lpddr4_rtl_1_dq_a[2]
BH5	lpddr4_rtl_1_dq_a[3]
BG4	lpddr4_rtl_1_dq_a[4]
BH3	lpddr4_rtl_1_dq_a[5]
BG3	lpddr4_rtl_1_dq_a[6]
BK5	lpddr4_rtl_1_dq_a[7]
BE13	lpddr4_rtl_1_dq_a[8]
BD11	lpddr4_rtl_1_dq_a[9]
BJ13	lpddr4_rtl_1_dq_b[0]
BF9	lpddr4_rtl_1_dq_b[1]
BB2	lpddr4_rtl_1_dq_b[10]
BE4	lpddr4_rtl_1_dq_b[11]
BE5	lpddr4_rtl_1_dq_b[12]
BE3	lpddr4_rtl_1_dq_b[13]
BE2	lpddr4_rtl_1_dq_b[14]
BD5	lpddr4_rtl_1_dq_b[15]
BH11	lpddr4_rtl_1_dq_b[2]
BF10	lpddr4_rtl_1_dq_b[3]
BH10	lpddr4_rtl_1_dq_b[4]
BJ11	lpddr4_rtl_1_dq_b[5]
BJ12	lpddr4_rtl_1_dq_b[6]
BK12	lpddr4_rtl_1_dq_b[7]
BC1	lpddr4_rtl_1_dq_b[8]

Table 21 : All ACAP Pins (continued on next page)

ACAP Pin	Signal
BD1	lpddr4_rtl_1_dq_b[9]
BL4	lpddr4_rtl_1_dqs_c_a[0]
BE10	lpddr4_rtl_1_dqs_c_a[1]
BF12	lpddr4_rtl_1_dqs_c_b[0]
BC5	lpddr4_rtl_1_dqs_c_b[1]
BK4	lpddr4_rtl_1_dqs_t_a[0]
BD10	lpddr4_rtl_1_dqs_t_a[1]
BF13	lpddr4_rtl_1_dqs_t_b[0]
BC6	lpddr4_rtl_1_dqs_t_b[1]
AV5	lpddr4_rtl_1_reset_n[0]
BT9	lpddr4_rtl_2_ca_a[0]
BT10	lpddr4_rtl_2_ca_a[1]
BP10	lpddr4_rtl_2_ca_a[2]
BV9	lpddr4_rtl_2_ca_a[3]
BM11	lpddr4_rtl_2_ca_a[4]
BN10	lpddr4_rtl_2_ca_a[5]
BP8	lpddr4_rtl_2_ca_b[0]
BU8	lpddr4_rtl_2_ca_b[1]
BN8	lpddr4_rtl_2_ca_b[2]
BM8	lpddr4_rtl_2_ca_b[3]
BR8	lpddr4_rtl_2_ca_b[4]
BR9	lpddr4_rtl_2_ca_b[5]
BL11	lpddr4_rtl_2_ck_c_a[0]
BN9	lpddr4_rtl_2_ck_c_b[0]
BL12	lpddr4_rtl_2_ck_t_a[0]
BM9	lpddr4_rtl_2_ck_t_b[0]
BL10	lpddr4_rtl_2_cke_a[0]
BL9	lpddr4_rtl_2_cke_a[1]
BU9	lpddr4_rtl_2_cke_b[0]
BP7	lpddr4_rtl_2_cke_b[1]
BV10	lpddr4_rtl_2_cs_a[0]
BR10	lpddr4_rtl_2_cs_a[1]
BR3	lpddr4_rtl_2_cs_b[0]
BT5	lpddr4_rtl_2_cs_b[1]
BK13	lpddr4_rtl_2_dmi_a[0]
BR5	lpddr4_rtl_2_dmi_a[1]

Table 21 : All ACAP Pins (continued on next page)

ACAP Pin	Signal
BU12	lpddr4_rtl_2_dmi_b[0]
BR4	lpddr4_rtl_2_dmi_b[1]
BG15	lpddr4_rtl_2_dq_a[0]
BF15	lpddr4_rtl_2_dq_a[1]
BN4	lpddr4_rtl_2_dq_a[10]
BN5	lpddr4_rtl_2_dq_a[11]
BT6	lpddr4_rtl_2_dq_a[12]
BV5	lpddr4_rtl_2_dq_a[13]
BU6	lpddr4_rtl_2_dq_a[14]
BV6	lpddr4_rtl_2_dq_a[15]
BE14	lpddr4_rtl_2_dq_a[2]
BH15	lpddr4_rtl_2_dq_a[3]
BM12	lpddr4_rtl_2_dq_a[4]
BM13	lpddr4_rtl_2_dq_a[5]
BM14	lpddr4_rtl_2_dq_a[6]
BL14	lpddr4_rtl_2_dq_a[7]
BM3	lpddr4_rtl_2_dq_a[8]
BM4	lpddr4_rtl_2_dq_a[9]
BU11	lpddr4_rtl_2_dq_b[0]
BV13	lpddr4_rtl_2_dq_b[1]
BP1	lpddr4_rtl_2_dq_b[10]
BN1	lpddr4_rtl_2_dq_b[11]
BN3	lpddr4_rtl_2_dq_b[12]
BP3	lpddr4_rtl_2_dq_b[13]
BU4	lpddr4_rtl_2_dq_b[14]
BT4	lpddr4_rtl_2_dq_b[15]
BV11	lpddr4_rtl_2_dq_b[2]
BV14	lpddr4_rtl_2_dq_b[3]
BR12	lpddr4_rtl_2_dq_b[4]
BR13	lpddr4_rtl_2_dq_b[5]
BT12	lpddr4_rtl_2_dq_b[6]
BT11	lpddr4_rtl_2_dq_b[7]
BR2	lpddr4_rtl_2_dq_b[8]
BP2	lpddr4_rtl_2_dq_b[9]
BD15	lpddr4_rtl_2_dqs_c_a[0]
BP5	lpddr4_rtl_2_dqs_c_a[1]

Table 21 : All ACAP Pins (continued on next page)

ACAP Pin	Signal
BP13	lpddr4_rtl_2_dqs_c_b[0]
BM1	lpddr4_rtl_2_dqs_c_b[1]
BD14	lpddr4_rtl_2_dqs_t_a[0]
BP6	lpddr4_rtl_2_dqs_t_a[1]
BP12	lpddr4_rtl_2_dqs_t_b[0]
BM2	lpddr4_rtl_2_dqs_t_b[1]
BR7	lpddr4_rtl_2_reset_n[0]
BV19	lpddr4_rtl_3_ca_a[0]
BV18	lpddr4_rtl_3_ca_a[1]
BV21	lpddr4_rtl_3_ca_a[2]
BV20	lpddr4_rtl_3_ca_a[3]
BT19	lpddr4_rtl_3_ca_a[4]
BT20	lpddr4_rtl_3_ca_a[5]
BJ20	lpddr4_rtl_3_ca_b[0]
BJ21	lpddr4_rtl_3_ca_b[1]
BM22	lpddr4_rtl_3_ca_b[2]
BK22	lpddr4_rtl_3_ca_b[3]
BJ22	lpddr4_rtl_3_ca_b[4]
BL22	lpddr4_rtl_3_ca_b[5]
BU17	lpddr4_rtl_3_ck_c_a[0]
BH21	lpddr4_rtl_3_ck_c_b[0]
BT17	lpddr4_rtl_3_ck_t_a[0]
BH20	lpddr4_rtl_3_ck_t_b[0]
BT21	lpddr4_rtl_3_cke_a[0]
BU19	lpddr4_rtl_3_cke_a[1]
BK18	lpddr4_rtl_3_cke_b[0]
BJ18	lpddr4_rtl_3_cke_b[1]
BU18	lpddr4_rtl_3_cs_a[0]
BU21	lpddr4_rtl_3_cs_a[1]
BP20	lpddr4_rtl_3_cs_b[0]
BF21	lpddr4_rtl_3_cs_b[1]
BN20	lpddr4_rtl_3_dmi_a[0]
BD17	lpddr4_rtl_3_dmi_a[1]
BE20	lpddr4_rtl_3_dmi_b[0]
BT15	lpddr4_rtl_3_dmi_b[1]
BR22	lpddr4_rtl_3_dq_a[0]

Table 21 : All ACAP Pins (continued on next page)

ACAP Pin	Signal
BT22	lpddr4_rtl_3_dq_a[1]
BF16	lpddr4_rtl_3_dq_a[10]
BJ16	lpddr4_rtl_3_dq_a[11]
BM17	lpddr4_rtl_3_dq_a[12]
BL17	lpddr4_rtl_3_dq_a[13]
BH16	lpddr4_rtl_3_dq_a[14]
BG17	lpddr4_rtl_3_dq_a[15]
BP22	lpddr4_rtl_3_dq_a[2]
BP21	lpddr4_rtl_3_dq_a[3]
BP18	lpddr4_rtl_3_dq_a[4]
BR20	lpddr4_rtl_3_dq_a[5]
BR19	lpddr4_rtl_3_dq_a[6]
BP17	lpddr4_rtl_3_dq_a[7]
BJ15	lpddr4_rtl_3_dq_a[8]
BE16	lpddr4_rtl_3_dq_a[9]
BD20	lpddr4_rtl_3_dq_b[0]
BF19	lpddr4_rtl_3_dq_b[1]
BU16	lpddr4_rtl_3_dq_b[10]
BV16	lpddr4_rtl_3_dq_b[11]
BV15	lpddr4_rtl_3_dq_b[12]
BU14	lpddr4_rtl_3_dq_b[13]
BR15	lpddr4_rtl_3_dq_b[14]
BR14	lpddr4_rtl_3_dq_b[15]
BG20	lpddr4_rtl_3_dq_b[2]
BF22	lpddr4_rtl_3_dq_b[3]
BG21	lpddr4_rtl_3_dq_b[4]
BF18	lpddr4_rtl_3_dq_b[5]
BE22	lpddr4_rtl_3_dq_b[6]
BD21	lpddr4_rtl_3_dq_b[7]
BT14	lpddr4_rtl_3_dq_b[8]
BP16	lpddr4_rtl_3_dq_b[9]
BR18	lpddr4_rtl_3_dqs_c_a[0]
BK17	lpddr4_rtl_3_dqs_c_a[1]
BE19	lpddr4_rtl_3_dqs_c_b[0]
BP15	lpddr4_rtl_3_dqs_c_b[1]
BR17	lpddr4_rtl_3_dqs_t_a[0]

Table 21 : All ACAP Pins (continued on next page)

ACAP Pin	Signal
BJ17	lpddr4_rtl_3_dqs_t_a[1]
BD18	lpddr4_rtl_3_dqs_t_b[0]
BN15	lpddr4_rtl_3_dqs_t_b[1]
BT7	lpddr4_rtl_3_reset_n[0]
AU6	MEM_CLK_0_PIN_N
AT6	MEM_CLK_0_PIN_P
BM7	MEM_CLK_1_PIN_N
BL7	MEM_CLK_1_PIN_P
B27	MODE0
B28	MODE1
B29	MODE2
C28	MODE3
BF57	MP01_RD_BUFF
BE57	MP01_TD_BUFF
BE55	MP02_RD_BUFF
BE54	MP02_TD_BUFF
BF54	nEN_MP_BUFF
G5	OMFP0_C2M_DP0_N
H5	OMFP0_C2M_DP0_P
J6	OMFP0_C2M_DP1_N
K6	OMFP0_C2M_DP1_P
G7	OMFP0_C2M_DP2_N
H7	OMFP0_C2M_DP2_P
J8	OMFP0_C2M_DP3_N
K8	OMFP0_C2M_DP3_P
D4	OMFP0_M2C_DP0_N
E4	OMFP0_M2C_DP0_P
B5	OMFP0_M2C_DP1_N
C5	OMFP0_M2C_DP1_P
D6	OMFP0_M2C_DP2_N
E6	OMFP0_M2C_DP2_P
B7	OMFP0_M2C_DP3_N
C7	OMFP0_M2C_DP3_P
G9	OMFP1_C2M_DP0_N
H9	OMFP1_C2M_DP0_P
J10	OMFP1_C2M_DP1_N

Table 21 : All ACAP Pins (continued on next page)

ACAP Pin	Signal
K10	OMFP1_C2M_DP1_P
G11	OMFP1_C2M_DP2_N
H11	OMFP1_C2M_DP2_P
J12	OMFP1_C2M_DP3_N
K12	OMFP1_C2M_DP3_P
D8	OMFP1_M2C_DP0_N
E8	OMFP1_M2C_DP0_P
B9	OMFP1_M2C_DP1_N
C9	OMFP1_M2C_DP1_P
D10	OMFP1_M2C_DP2_N
E10	OMFP1_M2C_DP2_P
B11	OMFP1_M2C_DP3_N
C11	OMFP1_M2C_DP3_P
G13	OMFP2_C2M_DP0_N
H13	OMFP2_C2M_DP0_P
J14	OMFP2_C2M_DP1_N
K14	OMFP2_C2M_DP1_P
G15	OMFP2_C2M_DP2_N
H15	OMFP2_C2M_DP2_P
J16	OMFP2_C2M_DP3_N
K16	OMFP2_C2M_DP3_P
D12	OMFP2_M2C_DP0_N
E12	OMFP2_M2C_DP0_P
B13	OMFP2_M2C_DP1_N
C13	OMFP2_M2C_DP1_P
D14	OMFP2_M2C_DP2_N
E14	OMFP2_M2C_DP2_P
B15	OMFP2_M2C_DP3_N
C15	OMFP2_M2C_DP3_P
G46	OMFP3_C2M_DP0_N
H46	OMFP3_C2M_DP0_P
J47	OMFP3_C2M_DP1_N
K47	OMFP3_C2M_DP1_P
G48	OMFP3_C2M_DP2_N
H48	OMFP3_C2M_DP2_P
J49	OMFP3_C2M_DP3_N

Table 21 : All ACAP Pins (continued on next page)

ACAP Pin	Signal
K49	OMFP3_C2M_DP3_P
D47	OMFP3_M2C_DP0_N
E47	OMFP3_M2C_DP0_P
B48	OMFP3_M2C_DP1_N
C48	OMFP3_M2C_DP1_P
D49	OMFP3_M2C_DP2_N
E49	OMFP3_M2C_DP2_P
B50	OMFP3_M2C_DP3_N
C50	OMFP3_M2C_DP3_P
G42	OMFP4_C2M_DP0_N
H42	OMFP4_C2M_DP0_P
J43	OMFP4_C2M_DP1_N
K43	OMFP4_C2M_DP1_P
G44	OMFP4_C2M_DP2_N
H44	OMFP4_C2M_DP2_P
J45	OMFP4_C2M_DP3_N
K45	OMFP4_C2M_DP3_P
D43	OMFP4_M2C_DP0_N
E43	OMFP4_M2C_DP0_P
B44	OMFP4_M2C_DP1_N
C44	OMFP4_M2C_DP1_P
D45	OMFP4_M2C_DP2_N
E45	OMFP4_M2C_DP2_P
B46	OMFP4_M2C_DP3_N
C46	OMFP4_M2C_DP3_P
J41	OMFP5_C2M_DP0_N
K41	OMFP5_C2M_DP0_P
G40	OMFP5_C2M_DP1_N
H40	OMFP5_C2M_DP1_P
J39	OMFP5_C2M_DP2_N
K39	OMFP5_C2M_DP2_P
G38	OMFP5_C2M_DP3_N
H38	OMFP5_C2M_DP3_P
B42	OMFP5_M2C_DP0_N
C42	OMFP5_M2C_DP0_P
D41	OMFP5_M2C_DP1_N

Table 21 : All ACAP Pins (continued on next page)

ACAP Pin	Signal
E41	OMFP5_M2C_DP1_P
B40	OMFP5_M2C_DP2_N
C40	OMFP5_M2C_DP2_P
D39	OMFP5_M2C_DP3_N
E39	OMFP5_M2C_DP3_P
BP56	OPT_SCL_1V5
BP55	OPT_SDA_1V5
Y8	OPTCLK0_N
Y9	OPTCLK0_P
R10	OPTCLK1_N
R11	OPTCLK1_P
AA49	OPTCLK2_N
AA48	OPTCLK2_P
U49	OPTCLK3_N
U48	OPTCLK3_P
F27	PCIE_RST_1V8_L
E27	PCIE_RST_1V8_L
AU12	PCIECLK0_N
AU13	PCIECLK0_P
AK8	PCIECLK1_N
AK9	PCIECLK1_P
BA45	PCIECLK2_N
BA44	PCIECLK2_P
AE49	PCIECLK3_N
AE48	PCIECLK3_P
BP58	PERST_PL_L
H26	PMC_SMON_SCL
G26	PMC_SMON_SDA
AW19	POR_B
U10	PROGCLK0_N
U11	PROGCLK0_P
N10	PROGCLK1_N
N11	PROGCLK1_P
W49	PROGCLK2_N
W48	PROGCLK2_P
AB8	PROGCLK3_N

Table 21 : All ACAP Pins (continued on next page)

ACAP Pin	Signal
AB9	PROGCLK3_P
C29	PUDC_B
H25	QSPI0_CLK
N24	QSPI0_CS_b
N25	QSPI0_IO[0]
J25	QSPI0_IO[1]
K25	QSPI0_IO[2]
L25	QSPI0_IO[3]
H23	QSPI1_CLK
L24	QSPI1_CS_b
K24	QSPI1_IO[0]
H24	QSPI1_IO[1]
G24	QSPI1_IO[2]
G23	QSPI1_IO[3]
BG58	REFCLK_FABRIC_N
BG57	REFCLK_FABRIC_P
AN16	REFCLK33M0_PS
A29	RTC_PADI
A30	RTC_PADO
E29	SDIO_CLK
M29	SDIO_CMD
N29	SDIO_DAT0
N28	SDIO_DAT1
M28	SDIO_DAT2
K28	SDIO_DAT3
J28	SDIO_SEL
BJ56	SI5344_IN0_N
BJ55	SI5344_IN0_P
BK54	SI5344_INTR_1V5_N
BD58	SI5344_LOL_1V5_N
BE58	SI5344_LOL_XAXB_1V5_N
BK55	SI5344_RST_1V5_N
BK57	SI5344_SCL_1V5
BJ57	SI5344_SDA_1V5
BN56	SRVC_MD_L_1V5
BG56	SW_USR0

Table 21 : All ACAP Pins (continued on next page)

ACAP Pin	Signal
BG54	SW_USR1
BH54	SW_USR2
K27	UART0_RXD
L27	UART0_TXD
BL57	VPX_AUXCLK_XPIO_N
BK58	VPX_AUXCLK_XPIO_P
BN55	VPX_CLK1_1V5
BM56	VPX_GDISC1#_BUF
BM57	VPX_GPIO1_INBUF
BM58	VPX_GPIO1_OUTn
BL54	VPX_nMSKRST_BUF
BN54	VPX_REFCLK_XPIO_N
BM54	VPX_REFCLK_XPIO_P

Table 21 : All ACAP Pins

Revision History

Date	Revision	Nature of Change
3rd December 2025	0.1	Initial Draft
15th July 2026	0.2	Updated board image
28th July 2026	1.0	First Release

Address: 160 Dundee Street,
Edinburgh, EH11 1DQ, UK
Telephone: +44 131 558 2600
Email: sales@alpha-data.com
Website: http://www.alpha-data.com

Address: 10822 West Toller Drive, Suite 120,
Deer Creek Technology Center, Littleton, CO 80127
Telephone: (303) 954 8768
Email: sales@alpha-data.com
Website: http://www.alpha-data.com